WHAT IS CLAIMED IS:

1. A variable dividing circuit comprising:

a shift register configured by cascade connection of D-type flip-flops with an initializing means by clock synchronization; and

a selecting means for selecting any one of output signals at respective stages of said shift register;

wherein said variable dividing circuit initializes each stage of said D-type flip-flops.

2. The variable dividing circuit according to claim 1,

wherein an H level signal is inputted in a first stage of said D-type flip-flop;

said initializing means comprises a reset means; and

said selecting means comprises a multiplexer.

3. The variable dividing circuit according to claim 1,

wherein an H level signal is inputted in a first stage of said D-type flip-flop;

said initializing means comprises a reset means; and

said selecting means comprises a switch circuit.

4. The variable dividing circuit according to claim 1,

wherein an L level signal is inputted in a first stage of said D-type flip-flop;

said initializing means comprises a preset means; and

said selecting means comprises a multiplexer.

5. The variable dividing circuit according to claim 1,

wherein an L level signal is inputted in a first stage of said D-type flip-flop;

said initializing means comprises a preset means; and

said selecting means comprises a switch circuit.